Topics

Updates

- Specifications
- VFB (VA Frontend Board)
- VARC (VA Readout Controller)
  - Time Stamping
  - Clock receiver/emulator
  - VME Interface / VME Crate specs
  - Sparsification
- VMM (VARC Mezzanine Module)

Oct 99 Review followup

- Hardware vs Software trigger
- Calibration issues
- VA Pedestal drift, stability, common mode noise, etc
- Time stamping
- Other

Schedule

- VA-DAQ tests
- Prototype electronics
- Production
- Installation / prototype electronics at Soudan

Oct 99 Review issues (Not exhaustive list)

- **Hardware vs Software trigger (J.Dawson, B. Foster, R. Tschirhart, ..)**
  - **Far detector is dominated by singles (< 1 kHz/PMT)**
  - **1 Hz cosmics used for calibration → must be near live between spills.**
  - **Software (processor farm) is adequate to trigger cosmics, neutrino events, …..**
  - **Hardware trigger would require engineering effort with no obvious benefit.**
  - **Software trigger is long standing MINOS Far Detector decision**
- **Calibration strategy (A. Para, J. Dawson, …)**
- **Timestamp improvements (B. Foster, ..)**
- **"Electrical" issues**
  - **Grounding, shielding, pickup, etc.**
  - **HV Ground loop isolation, ground resistors (K. Lang)**
  - **Clock signal skew in VME crate (B. Foster)**
  - **VA chip bias uniformity (J. Cobb)**
  - **Analog cable dispersion & settling : Would we benefit from cable equalizers? (B. Foster)**
  - **Other electrical issues…**
- **Other..**

Specifications

PMT Anode signal

- **Nominal gain** **1e6 (minimum gain 0.5e6) ie**

  →**<=***2:1 pixel gain spread among all 3 PMTs in a MuxBox*

- **Single pe charge** **160 fc (80 fc min)**
- **Full scale charge** **150 pe , 24 pc (12 pc min)**
- **ADC resolution** **14 bits (16k counts)**
- **ADC scaling** **1 ADC count = 1.5 fc**
- **"** **1 pe = 106 (53 min)**
- **enc (thermal)** **~< 1fc, < 1 ADC count**
- **pedestal width** **2 – 4 counts (* Discussion follows)**
- **"** **2% - 4% pe (nominal) 4%-8% (wc)**

PMT Dynode signal (ASD-lite)

- **Nominal gain** **500e3 (250e3) {(Gd-1)/Gd}*Ganode**
- **Single pe** **80 fc (40 fc min)**
- **enc (ASD-lite)** **~1/2 fc**
- **SNR** **80 min**
- **Output** **LVDS**

VFB update

- **3" x 8" card**
- **(3) VA Chips**
- **4-channel dynode trigger (ASD-lite); Tests in progress (Roy Lee)**
- **Programmable VA bias via serial slo-control**
- **(3) PIN Diodes/amplifiers**
  - **Circuits prototyped (P. Smith - Sussex)**
  - **up to 20x gain**
  - **enc << 1 fc (See P. Smith for details)**
  - **inexpensive dual opamp (OPA2350) 5nv/rt(Hz), ft=38 MHz, single supply – rail-to-rail (5V)**
- **Schematics complete (Phil Sullivan - Oxford)**
- **Layout in progress (Phil Sullivan)**
- **Mux-box interface conceptual (and physical) design (U. Texas, U. Indiana) near complete**

VARC Update

- **(6) VMMs per VARC – 1 VMM per 2 VFBs**
  - **VMM : Dual VA Receiver**
  - **14 bit, 10 MHz ADC (Analog Devices)**
  - **+/- 5V low dropout regulators for power supply noise isolation**
  - **All analog components on VMM, none on VARC.**
- **Timestamp resolution enhancement 3.125 ns → 1.5 ns (Nathan Felt)**
- **VME interface / Crate Spec (Nathan)**
- **VA common mode noise, cm noise suppression (Roy Lee)**

Prototypes in 2000 : Components purchased for

- **5 VARCs**
- **15 VMMs**
- **30 VFBs**
- **30 Cable sets; Power, Control, Analog**

- **Soudan Installation & checkout personnel**
- **~ 1 FTE**
  - **Roy Lee – Post Doc**
  - **Mark Szigety – Graduate student**
  - **Andre Lebedev – Graduate student**
  - **Nathan Felt – Engineer**
  - **John Oliver - Engineer**